What is claimed is:

1. A fast latch comprising:

a NAND stage adapted to receive a clock signal and a data input signal;

a clocked inverter stage, a first input of said clocked inverter stage coupled to the output of said NAND stage and a second input of said clocked inverter stage coupled to said clock signal;

a first inverter stage, a first input of said first inverter stage coupled to an output of said clocked inverter stage and a second input of said first inverter stage coupled to a reset signal; and

a second inverter stage having an output, an input of said second inverter stage coupled to an output of said first inverter stage.

2. The fast latch of claim 1, wherein said reset signal is coupled to a gate of an FET, source/drains of said FET coupled between ground and said input of said first inverter stage.

3. The fast latch of claim 1, wherein a logical one on said reset signal drives said output of said fast latch to a logical zero.

4. The fast latch of claim 1, wherein a logical zero on said reset signal and a logical zero on said clock signal precharges said output of said NAND stage to a logical one.

5. The fast latch of claim 1, wherein a logical one on said clock signal and a logical one on said data input signal drives said output of said NAND stage to a logical 0, drives said output of said clocked inverter to a logical one and drives said output of said fast latch to a logical one.

6. The fast latch of claim 1, wherein a logical one on said clock signal and a logical zero on said data input leaves said output of said NAND stage at a precharged state of a logical one, drives said output of said clocked inverter to a logical zero and drives said output of said second inverter to a logical zero.

7. The fast latch of claim 1, wherein said NAND stage and said clocked inverter stage have a latch capture time defined as one divided by twice the sum a maximum frequency operating frequency of the combination of said NAND stage, said clocked inverter stage, said first inverter stage and said second inverter stage.

8. The fast latch of claim 1, wherein said NAND stage and said clocked inverter stage have a latch capture time of 100 pico seconds or less.

9. The fast latch of claim 1, wherein said clock signal has a frequency of up to 4.545 GHz.

10. A frequency divider generating an output clock signal, comprising:

a one-shot generator, an input of said one-shot generator coupled to an input clock signal and an output of said one shot generator coupled to clock inputs of at least two latches, said latches arranged as a shift register, a data output of a previous latch of said shift register coupled to a data input of a following latch of said shift register and a data output of a last latch of said shift register coupled to a data input of a first latch of said shift register;

an output of said frequency divider coupled to the output of a next to last latch of said shift register; and

wherein, the frequency of said output clock signal is a function of the frequency of said input clock signal and the number of said latches.

11. The frequency divider of claim 10, further including:

a logic network responsive to a control signal, said logic network coupled to the data output of a next to last latch of said shift register and to the data output said last latch and the data input of said first latch; and

said logic network, based on a value of said control signal, either further coupling the data output of said next to last latch to the data input of said first latch or only coupling the data output of said last latch to the data input of said first latch.

12. The frequency divider of claim 11, wherein:

the frequency of said output clock signal when said control signal has a first value is the frequency of said input clock signal divided a first number, said first number equal to twice the number of latches in said shift register, and

the frequency of said output clock signal when said control signal has a second value is the frequency of said input clock signal divided by a second number, said second number equal to one less than said first number.

13. The frequency divider circuit of claim 11, further comprising a output clock duty cycle correction circuit coupled between the output of said next to last latch and the output of said frequency divider.

14. The frequency divider of claim 13, wherein said output clock duty cycle correction circuit is adapted to correct only output clock frequencies where the ratio of the input clock frequency divided by the output clock frequency is an odd number and based upon an additional control signal.

15. The frequency divider of claim 10, further including additional one-shot generators, the input of said additional on-shot generators coupled to the output of said inverting multiplexer and the outputs of said one-shot generator and each additional one-shot generator connected to the clock input of different latches.

16. The frequency divider of claim 10, wherein all said latches comprise:

a NAND stage adapted to receive said input clock signal and a data input signal from a previous latch;

a clocked inverter stage, a first input of said clocked inverter stage coupled to the output of said NAND stage and a second input of said clocked inverter stage coupled to said clock signal;

a first inverter stage, a first input of said first inverter stage coupled to an output of said clocked inverter stage and a second input of said first inverter stage coupled to a reset signal; and

a second inverter stage, an input of said first inverter stage coupled to an output of said first inverter stage, an output of said second inverter stage being the data output of said latch.

17. A programmable frequency divider, comprising:

a multiplicity of frequency dividers each generating a different output clock signal, each comprising:

a one-shot generator, an input of said one-shot generator coupled to an input clock signal and an output of said one shot generator coupled to clock inputs of at least two latches, said latches arranged as a shift register, a data output of a previous latch of said shift register coupled to a data input of a following latch of said shift register and a data output of a last latch of said shift register coupled to a data input of a first latch of said shift register;

an output of said frequency divider coupled to the output of a next to last latch of said shift register; and

wherein, the frequency of each output clock signal is a function of the frequency of said input clock signal and the number of said latches in each frequency divider;

wherein the number of latches in each frequency divider is different;

means for generating a different reset signal for each frequency divider; and

means for selecting and coupling one said output clock signal of one said frequency divider to a clock output of said programmable divider.

18. The programmable frequency divider of claim 17, wherein each frequency divider further includes:

a logic network responsive to a common control signal, said logic network coupled to the data output of a next to last latch of said shift register and to the data output said last latch and the data input of said first latch; and

said logic network, based on a value of said common control signal, either further coupling the data output of said next to last latch to the data input of said first latch or only coupling the data output of said last latch to the data input of said first latch.

19. The programmable frequency divider of claim 18, wherein:

the frequency of said output clock signal when said control signal has a first value is the frequency of said input clock signal divided a first number, said first number equal to twice the number of latches in said shift register, and

the frequency of said output clock signal when said control signal has a second value is the frequency of said input clock signal divided by a second number, said second number equal to one less than said first number.

20. The programmable frequency divider circuit of claim 18, wherein each frequency divider further comprises an output clock duty cycle correction circuit coupled between the output of said next to last latch and said output of said frequency divider.

21. The programmable frequency divider of claim 20, wherein said output clock duty cycle correction circuit of each frequency divider is adapted to correct only output clock

frequencies where the ratio of said input clock frequency divided by said output clock frequency is an odd number and is based upon an additional control signal.

22. The programmable frequency divider of claim 17, wherein each frequency divider further includes additional one-shot generators, the output of each one-shot generator connected to the clock input of different latches of each frequency divider.

23. The programmable frequency divider of claim 17, wherein all said latches of all said frequency dividers comprise:

a NAND stage adapted to receive said input clock signal and to receive a data input signal from a previous latch of said frequency divider;

a clocked inverter stage, a first input of said clocked inverter stage coupled to the output of said NAND stage and a second input of said clocked inverter stage coupled to said input clock signal;

a first inverter stage, a first input of said first inverter stage coupled to an output of said clocked inverter stage and a second input of said first inverter stage coupled to a reset signal; and

a second inverter stage having an output, an input of said first inverter stage coupled to an output of said first inverter stage.

24. The programmable frequency divider of claim 17, wherein one of said frequency dividers is a divide by two frequency divider and is a state machine.

25. The programmable frequency divider of claim 17, wherein one said frequency divider is a divide by 3 or 4 frequency divider, said 3 or 4 frequency divider including first and second identical circuits each comprising:

a one-shot generator, an input of said one-shot generator coupled to said input clock signal and an output of said one shot generated coupled to clock inputs of a first and a second latch, said first and second latches arranged as a shift register, a data output of said first latch coupled to a data input of said second latch and a data output of said second latch coupled to a data input of said first latch;

a logic network responsive to a control signal, said logic network coupled to the data output of a next to last latch of said shift register and to the data output said last latch and the data input of said first latch;

said logic network, based on a value of said control signal, either further coupling the data output of said next to last latch to the data input of said first latch or only coupling the data output of said last latch to the data input of said first latch; and

an additional logic network coupling outputs of said first and second circuits to a divide by 3 output or a divide by 4 output of said divide by 3 or 4 frequency divider.

26. A divide by 2 frequency divider comprising:

identical first set and second sets of cascaded of FETs, each set adapted to receive an input clock signal and an inverted version of said input clock signal; and

a first inverter, the gate of a PFET of said first inverter coupled to an output of said first set of cascaded FETs, the gate of an NFET of said first inverter coupled to an output of said second set of cascaded FETs, an output of said first inverter coupled to an output of said frequency divider and to inputs of said first and second sets of cascaded FETs.

27. The divide by 2 frequency divider of claim 26 further including:

a second inverter, an input of said second inverter coupled to the output of said second inverter and the output of said second inverter coupled to the input of a third inverter, the output of said third inverter coupled to said output of said frequency divider;

a first pass gate responsive to said inverted input clock signal coupled between the output of said second inverter and said first and second sets of cascaded FETs and a second pass gate responsive to said input clock signal coupled between the output of said second inverter and said first and second sets of cascaded FETs, said pass gates controlling feedback of said output of said first inverter to said first and second sets of cascaded FETs.

28. The divide by two frequency divider of claim 26, wherein each set of cascaded FETs includes, connected in the sequence recited, a first PFET connected to a positive power

source, a second PFET connected between said first PFET and a first NFET, a second NFET connected between said first NFET and ground, all connections being source, drain or source to drain connections.

29. The divide by two frequency divider of claim 28, wherein:

said first pass gate is a PFET and the second pass gate is an NFET, of which the first source/drain of each is connected to the output of said second inverter, the second source/drain of each is connected to gates of said first PFET and first NFET of said first set of cascaded FETs and to said second NFET and said second PFET of said second set of cascaded FETs, the gate of said first pass gate coupled to said inverted input clock signal and the gate of said second pass gate coupled to said clock signal;

the gates of said second PFET of said first set of cascaded FETs and said first PFET of said second set of cascaded FETS coupled to said input clock signal; and

the gates of said second NFET of said first set of cascaded FETs and said first NFET of said second set of cascaded FETS coupled to said inverted input clock signal.

30. The divide by two frequency divider of claim 29 further including:

a reset NFET, the source of said reset NFET coupled to ground, the drain of said reset NFET coupled to the output of said second inverter and the gate of said reset NFET coupled to a reset signal.